ABSTRACT OF THE DISCLOSURE

An electrically programmable and erasable non-volatile semiconductor memory such as a flash memory is designed into a configuration in which, when a cutoff of the power supply occurs in the course of a write or erase operation carried out on a memory cell employed in the non-volatile semiconductor memory, the operation currently being executed is discontinued and a write-back operation is carried out to change a threshold voltage of the memory cell in the reversed direction. In addition, the configuration also allows the number of charge-pump stages in an internal power-supply configuration to be changed in accordance with the level of a power-supply voltage so as to make the write-back operation correctly executable. As a result, no memory cells are put in deplete state even in the event of a power-supply cutoff in the course of a write or erase operation.